DOCKET NO.: TIC-0067 **Application No.:** 10/500,065

Office Action Dated: January 12, 2006

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A noise removing circuit, comprising: a highpass filter for detecting a noise component included in an input signal; an amplifier for amplifying the noise component output from the highpass filter; a time constant circuit for smoothing the amplified noise component with a predetermined time constant and for generating a control voltage that is applied to the amplifier, wherein said time constant circuit comprises:

a first capacitor;

a charge circuit for charging the first capacitor;

a discharge circuit for discharging the first capacitor; and

a charge/discharge speed setting unit that causes a difference between a charge speed of the charge circuit and a discharge speed of the discharge circuit;

a pulse generating circuit <u>for</u> generating a pulse having a predetermined width at timing when a voltage level of the noise component output from said highpass filter becomes a predetermined reference voltage or higher;

an analog delaying circuit <u>for</u> delaying the input signal by a predetermined amount of time, and <u>for</u> outputting the delayed signal; and

an outputting circuit <u>for</u> holding the signal output from said analog delaying circuit at immediately preceding timing when the pulse generated by said pulse generating circuit is input, and <u>for</u> outputting the signal output from said analog delaying circuit unchanged in other cases, wherein said analog delaying circuit comprises:

a plurality of second capacitors;

a plurality of first switches <u>for</u> making said plurality of <u>second</u> capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to the plurality of <u>second</u> capacitors in a predetermined order at different timing; and

a plurality of second switches <u>for</u> extracting the voltage of the input signal respectively held by said plurality of <u>second</u> capacitors before next timing when the voltage is held is reached.

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(Currently amended) A noise removing circuit, comprising:

 a noise extracting circuit <u>for extracting a noise component included in an input signal;
 an amplifier circuit for amplifying the noise component output from the noise extracting circuit;

</u>

a time constant circuit for smoothing the amplified noise component with a predetermined time constant and for generating a control voltage that is applied to the amplifier circuit, wherein said time constant circuit comprises:

a first capacitor;

a charge circuit for charging the first capacitor;

a discharge circuit for discharging the first capacitor; and

a charge/discharge speed setting unit that causes a difference between a charge speed of the charge circuit and a discharge speed of the discharge circuit;

a pulse generating circuit <u>for</u> generating a pulse having a predetermined width at timing when a voltage level of the noise component output from said noise extracting circuit becomes a predetermined reference voltage or higher;

an analog delaying circuit having comprising:

a plurality of second capacitors;

a plurality of first switches <u>for making said plurality of second</u> capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to said plurality of <u>second</u> capacitors in a predetermined order at different timing; and

a plurality of second switches <u>for</u> making said plurality of <u>second</u> capacitors output the voltage of the input signal respectively held by said plurality of <u>second</u> capacitors in a predetermined order at timing delayed by a predetermined amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit; and

an outputting circuit <u>for</u> holding the signal output from said analog delaying circuit at immediately preceding timing when the pulse having the predetermined width is output from said pulse generating circuit, and <u>for</u> outputting the signal output from said analog delaying circuit unchanged in other cases.

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3. (Currently amended) A noise removing circuit, comprising:
a noise extracting circuit for extracting a noise component included in an input signal;
an amplifier circuit for amplifying the noise component output from the noise extracting circuit;

a time constant circuit for smoothing the amplified noise component with a predetermined time constant and for generating a control voltage that is applied to the amplifier circuit, wherein said time constant circuit comprises:

- a first capacitor;
- a charge circuit for charging the first capacitor;
- a discharge circuit for discharging the first capacitor;
- a charge/discharge speed setting unit that causes a difference between a charge speed of the charge circuit and a discharge speed of the discharge circuit;

a pulse generating circuit <u>for generating</u> a pulse having a predetermined width at timing when a voltage level of the noise component output from said noise extracting circuit becomes a predetermined reference voltage or higher;

an analog delaying circuit having comprising:

a plurality of second capacitors;

a plurality of first switches <u>for</u> making said plurality of <u>second</u> capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to said plurality of <u>second</u> capacitors in a predetermined order at different timing; and

a plurality of second switches <u>for</u> making said plurality of <u>second</u> capacitors output the voltage of the input signal respectively held by said plurality of <u>second</u> capacitors in a predetermined order at timing delayed by a predetermined amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit; and

an outputting circuit <u>for</u> holding the signal output from said analog delaying circuit at immediately preceding timing when the pulse having the predetermined width is output from said pulse generating circuit, and <u>for</u> outputting the signal output from said analog delaying circuit unchanged in other cases, wherein

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all of said circuits are formed on a same semiconductor substrate with a MOS process.

4. (Previously Presented) The noise removing circuit according to claim 1, wherein

output terminals of said plurality of second switches are connected in common.

5. (Previously Presented) The noise removing circuit according to claim 1, wherein

said plurality of first switches are exclusively made electrically continuous.

6. (Previously Presented) The noise removing circuit according to claim 1, wherein

said plurality of second switches are exclusively made electrically continuous.

7. (Previously Presented) The noise removing circuit according to claim 1, wherein

each of said pluralities of first and second switches is an analog switch configured by connecting an FET of a p-channel type, and an FET of an n-channel type in parallel.

8. (Previously Presented) The noise removing circuit according to claim 1, wherein

said analog delaying circuit further comprises clock generating means for generating a clock signal that cyclically selects each of said plurality of first switches and said plurality of second switches.

9. (Original) The noise removing circuit according to claim 8, wherein said clock generating means supplies a clock signal, whose one cycle is an amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit, to said plurality of first switches and said plurality of second switches in a sequential order.

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- 10. (Currently amended) The noise removing circuit according to claim 1, wherein said analog delaying circuit further comprises an third output capacitor connected to each of said plurality of second capacitors via said plurality of second switches.
- 11. (Currently amended) The noise removing circuit according to claim 10, wherein

a capacitance of said <u>third</u> output capacitor is set to a value smaller than a capacitance of each of said plurality of <u>second</u> capacitors.

12. (Previously Presented) The noise removing circuit according to claim 1, wherein

constituent elements of the respective circuits are integrally formed on a semiconductor substrate.

13. (Previously Presented) The noise removing circuit according to claim 1, wherein

constituent elements of the respective circuits are integrally formed on a same semiconductor substrate with a CMOS process.